Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A memory device comprising:

a memory element including a layer of piezoelectric material and a layer of ferroelectric material, the two layers being separated by a common electrode and an input electrode being provided on one of the two layers and an output electrode being provided on the other of the two layers, the input and output electrodes being disposed on opposite sides of their respective layers compared with the common electrode, the two layers being clamped together such as to enhance the amplitude of a voltage generated across one of the two layers due to the application of a voltage to the other two layers; and

a comparator having a pair of inputs, the inputs being connected to the input and output electrodes, respectively, of the memory element, and an output for providing an indication of a logic state of the memory device, wherein the comparator compares a phase of a signal across the input and common electrodes with a phase of a signal across the output and common electrodes to provide said logic state indication.

2. (Original) A memory device as claimed in claim 1, wherein the piezoelectric material is a ferroelectric material.

3. (Previously Presented) A memory device as claimed in claim 1, wherein said clamping together is achieved by one of the following means: a means for maintaining a constant spacing between said input and output electrodes, and a means for exerting a constant force or stress upon one of the input and output electrodes relative to the other of the input and output electrodes.

4. (Previously Presented) A memory device as claimed in claim 2, wherein said clamping together is achieved by one of the following means: a means for maintaining a

constant spacing between said input and output electrodes, and a means for exerting a constant force or stress upon one of the input and output electrodes relative to the other of the input and output electrodes.

5. (Previously Presented) A memory arrangement comprising a plurality of devices as claimed in claim 1.

6. (Previously Presented) A memory arrangement as claimed in claim 5, wherein the respective input electrodes are arranged parallel to each other in a spaced apart manner in a first plane, the respective common electrodes are arranged parallel to each other in a spaced apart manner in a second plane and the respective output electrodes are arranged parallel to each other in a spaced apart manner in a third plane, with the said planes being parallel to each other, the input and output electrodes being parallel with each other and the common electrodes being perpendicular thereto.

7. (Withdrawn-Previously Presented) A method of data storage and retrieval comprising the steps of: providing a layer of ferroelectric material, providing a layer of piezoelectric material, clamping the two layers together, storing data by internally polarising the ferroelectric material in one of the two stable directions in accordance with the data to be stored, and retrieving stored data by applying a non-polarising voltage to one of the two layers and detecting a resultant voltage from the other of the two layers.

8. (Withdrawn-Original) A method as claimed in claim 7, wherein the step of providing a layer of piezoelectric material comprises the step of providing a ferroelectric material as that piezoelectric material.

9. (Withdrawn-Original) A method as claimed in claim 8, comprising the steps of: internally polarising the piezoelectric layer implemented by a ferroelectric material in a reference direction, arranging for the storage of data by internally polarisation in the said one of two directions relative to the reference direction.

10. (Withdrawn-Previously Presented) A method as claimed in claim 7, wherein the step of detecting the said resultant voltage comprising the phase of the said resultant voltage with the phase of the said applied non-polarising voltage.

11. (Canceled)

12. (Previously Amended) A memory arrangement comprising a plurality of devices as claimed in claim 2.

13. (Previously Amended) A memory arrangement comprising a plurality of devices as claimed in claim 3.

14. (Previously Amended) A memory arrangement comprising a plurality of devices as claimed in claim 4.

15. (Withdrawn-Previously Amended) A method as claimed in claim 8, wherein the step of detecting the said resultant voltage comprising the phase of the said resultant voltage with the phase of the said applied non-polarising voltage.

16. (Withdrawn-Previously Amended) A method as claimed in claim 9, wherein the step of detecting the said resultant voltage comprising the phase of the said resultant voltage with the phase of the said applied non-polarising voltage.

17. (Previously Presented) A memory arrangement as claimed in claim 12, wherein the respective input electrodes are arranged parallel to each other in a spaced apart manner in a first plane, the respective common electrodes are arranged parallel to each other in a spaced apart manner in a second plane and the respective output electrodes are arranged parallel to each other in a spaced apart manner in a third plane, with the said planes being parallel to each other, the input and output electrodes being parallel with each other and the common electrodes being perpendicular thereto.

18. (Previously Presented) A memory arrangement as claimed in claim 13, wherein the respective input electrodes are arranged parallel to each other in a spaced apart manner in

a first plane, the respective common electrodes are arranged parallel to each other in a spaced apart manner in a second plane and the respective output electrodes are arranged parallel to each other in a spaced apart manner in a third plane, with the said planes being parallel to each other, the input and output electrodes being parallel with each other and the common electrodes being perpendicular thereto.

19. (Previously Presented) A memory arrangement as claimed in claim 14, wherein the respective input electrodes are arranged parallel to each other in a spaced apart manner in a first plane, the respective common electrodes are arranged parallel to each other in a spaced apart manner in a second plane and the respective output electrodes are arranged parallel to each other in a spaced apart manner in a third plane, with the said planes being parallel to each other, the input and output electrodes being parallel with each other and the common electrodes being perpendicular thereto.

20. (Previously Presented) A memory device comprising:

a memory element including a layer of piezoelectric material and a layer of ferroelectric material, the two layers being separated by a common electrode and an input electrode being provided on one of the two layers and an output electrode being provided on the other of the layers, the input and output electrodes being disposed on opposite sides of their respective layers compared with the common electrode, the two layers being clamped together such as to enhance the amplitude of a voltage generated across one of the two layers due to the application of a voltage to the other two layers, said clamping together being achieved by one of the following means:

a means for maintaining a constant spacing between said input and output electrodes, and a means for exerting a constant force or stress upon one of the input and output electrodes relative to the other of the input and output electrodes.